IN THE SPECIFICATION

Please amend the paragraph beginning at page 1, line 3 is amended as follows:

This application is a Divisional of U.S. Application No. 09/505,018, filed February 16, 2000, now U.S. Patent No. 6,710,454, which is incorporated herein by reference.

Please delete the paragraphs beginning on page 3, line 22, starting with and including the heading, Summary of the Invention, through page 5, line 23, before the heading Brief Description of the Drawings.

Please insert the following paragraphs beginning on page 8, line 26 before the current paragraph beginning on page 8, line 26:

An electronic apparatus, in one embodiment, includes a first semiconductor device having a first side and an opposing second side. The first side of the first device includes a first array of connection pads. Also included is a flip chip adhesive layer covering the first side. The adhesive layer has a first array of openings extending through the layer where the first array of openings is substantially aligned with the first array of connection pads. The apparatus further includes an electrically conductive material substantially filling the first array of openings.

Another embodiment relates to a method of packaging a die at wafer level. The method includes applying a flip chip adhesive to a first side of a finished wafer, the wafer having at least one die thereon. An array of openings is then created in the adhesive. The array of openings provides access to an array of connection pads on each die. The array of openings is then substantially filled with an electrically conductive material.

In yet another embodiment, an electronic apparatus is provided having a first semiconductor device and a second semiconductor device. The first semiconductor device has a first side and a second side where the first side includes a first array of connection pads. The second semiconductor device also has a first side comprising a second array of connection pads. The second side of the first semiconductor device is coupled to the first side of the second semiconductor device such that the second array of connection pads is adjacent the first array of connection pads.

In still yet another embodiment, a semiconductor wafer is provided. The wafer includes

at least one die formed on a face of the wafer where the die has an array of connection pads electrically coupled to circuits on the die. Furthermore, the wafer includes an adhesive layer covering the face of the wafer. The adhesive layer has an array of openings where the array of openings are adapted to provide access to the array of connection pads.

A method of packaging two or more semiconductor devices is also provided. In this embodiment, a second side of a first semiconductor device is attached to a first side of a second semiconductor device such that a first array of connection pads located on a first side of the first semiconductor device is adjacent to a second array of electrical connection pads located on the first side of the second semiconductor device. An adhesive layer is applied over the first side of the first semiconductor device and the first side of the second semiconductor device.

An electronic system is provided in still yet another embodiment. The system includes a processor and a pre-packaged flip chip. The pre-packaged flip chip includes a first semiconductor device having a first side and a second side where the first side comprises a first array of connection pads. In addition, the pre-packaged flip chip includes a second semiconductor device also having a first side comprising a second array of connection pads. The second side of the first semiconductor device is coupled to the first side of the second semiconductor device such that the second array of connection pads is adjacent the first array of connection pads. An adhesive layer covers the first side of the first semiconductor device and the first side of the second semiconductor device. The adhesive layer has an array of openings substantially aligned with one or more connection pads of either the first array of connection pads or the second array of connection pads. A conductive material substantially fills the array of openings.

Further embodiments of the invention include apparatus and methods of varying scope.

Advantageously, the apparatus and methods of the various embodiments avoid time-consuming underfill operations by prepackaging a die or dice at wafer level. By packaging the die at wafer level, greater manufacturing efficiencies are obtainable due to simultaneous processing of multiple dice across the entire wafer face. In addition, various embodiments are also particularly amenable to pre-packaging multiple chips in a single module, permitting semiconductor packages having increased electronic densities. Since these multi-chip modules can also be packaged at wafer level, similar manufacturing economies are realized.